

L Number	Hits	Search Text	DB	Time stamp
16	627	(((((integrated adj1 circuit) or VLSI or LSI or IC) same (physical adj1 (design\$3 or model\$4 or simulati\$3))) or (((integrated adj1 circuit) or VLSI or LSI or IC) same layout)) and (((timing or delay\$3) same (error or fall\$3 or fail\$3)) same (threshold or edge or margin)))	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/12/17 14:27
17	6436	716/\$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/12/17 14:29
18	102	(((((integrated adj1 circuit) or VLSI or LSI or IC) same (physical adj1 (design\$3 or model\$4 or simulati\$3))) or (((integrated adj1 circuit) or VLSI or LSI or IC) same layout)) and (((timing or delay\$3) same (error or fall\$3 or fail\$3)) same (threshold or edge or margin))) and 716/\$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/12/17 14:29
19	550	((error or fall\$3 or fail\$3) with (threshold or edge or margin)) and ((((((integrated adj1 circuit) or VLSI or LSI or IC) same (physical adj1 (design\$3 or model\$4 or simulati\$3))) or (((integrated adj1 circuit) or VLSI or LSI or IC) same layout)) and (((timing or delay\$3) same (error or fall\$3 or fail\$3)) same (threshold or edge or margin))))	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/12/17 14:33
20	65	716/\$.ccls. and (((error or fall\$3 or fail\$3) with (threshold or edge or margin)) and ((((((integrated adj1 circuit) or VLSI or LSI or IC) same (physical adj1 (design\$3 or model\$4 or simulati\$3))) or (((integrated adj1 circuit) or VLSI or LSI or IC) same layout)) and (((timing or delay\$3) same (error or fall\$3 or fail\$3)) same (threshold or edge or margin))))	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/12/17 14:33
21	41	optimiz\$5 and (716/\$.ccls. and (((error or fall\$3 or fail\$3) with (threshold or edge or margin)) and ((((((integrated adj1 circuit) or VLSI or LSI or IC) same (physical adj1 (design\$3 or model\$4 or simulati\$3))) or (((integrated adj1 circuit) or VLSI or LSI or IC) same layout)) and (((timing or delay\$3) same (error or fall\$3 or fail\$3)) same (threshold or edge or margin))))	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/12/17 14:33
22	21	(logic\$4 with optimiz\$5) and (optimiz\$5 and (716/\$.ccls. and (((error or fall\$3 or fail\$3) with (threshold or edge or margin)) and ((((((integrated adj1 circuit) or VLSI or LSI or IC) same (physical adj1 (design\$3 or model\$4 or simulati\$3))) or (((integrated adj1 circuit) or VLSI or LSI or IC) same layout)) and (((timing or delay\$3) same (error or fall\$3 or fail\$3)) same (threshold or edge or margin))))	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/12/17 14:34

23	12	clock and ((logic\$4 with optimiz\$5) and (optimiz\$5 and (716/\$.ccls. and ((error or fall\$3 or fail\$3) with (threshold or edge or margin)) and (((((integrated adj1 circuit) or VLSI or LSI or IC) same (physical adj1 (design\$3 or model\$4 or simulati\$3))) or (((integrated adj1 circuit) or VLSI or LSI or IC) same layout)) and (((timing or delay\$3) same (error or fall\$3 or fail\$3)) same (threshold or edge or margin))))))	USPAT; US-PGPUB; EPO; JPO; DERWENT	2003/12/17 14:34
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